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EXAMINER	
CHEN, SHIN HON	

ART UNIT	PAPER NUMBER
2131	6

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No. 09/522,620	Applicant(s) POST ET AL.	
	Examiner Shin-Hon Chen	Art Unit 2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *July 3, 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3, 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-13 have been examined.

Oath/Declaration

2. The filing date and the application number were missing. Please make correction.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Sedlak et al. U.S. Pat. No. 6059191 (hereinafter Sedlak).

As per claim 1, Sedlak discloses a method for protecting a security module, in which security-relevant data are stored, inserted on a device motherboard (Sedlak: column2 lines 57-65 and figure 2), comprising the steps of monitoring proper insertion of said security module on said device motherboard with a first function unit (Sedlak: column 3 lines 8-10: triggering circuit), a second function unit (Sedlak: column 3 lines 3-5: sensor circuit) and a third function unit in said security module (Sedlak: column 3 lines 4-5: control circuit); detecting at least one of improper use and improper replacement of said security module with said second function unit and, upon a detection of at least one of said improper use and said improper replacement, said second function unit causing said security-relevant data to be erased (Sedlak: column 3 lines 8-11); during replacement of said security module, inhibiting functioning of said security module with said third function unit (Sedlak: column 30-46: the RAM memory requires a voltage supply); following at least one of proper use and proper replacement of said security module, re-initializing, with said first function unit any erased, security relevant data; and after said re-initializing, enabling each of said first function unit, said second function unit and said third function unit to re-commission said security module (Sedlak: column 3 lines 51-57).

As per claim 3, Sedlak further discloses a security module for insertion on a device motherboard (Sedlak: column 2 lines 57-65 and figure 2), comprising: a memory in which security-relevant data are stored (Sedlak: column 4 lines 3-24); voltage monitoring unit which supplies an operating voltage to said memory to maintain said security-relevant data stored therein and which disconnects said memory from said voltage, thereby erasing said security-relevant data therein, upon occurrence of a voltage level indicating at least one of improper use and replacement (Sedlak: column 4 lines 24-32 and column 3 lines 3-12); an

unplugged status detection unit which inhibits functioning of said security module during replacement of said security module and which has a self-holding capability, indicating that said security module has been replaced, which is triggered when a voltage level a test voltage line deviates from a predetermined voltage level (Sedlak: column 3 lines 1-39); and a processor connected to said voltage monitoring unit and to said unplugged status detection unit to re-commission said security module after at least one of said improper use and replacement, by enabling said voltage monitoring unit and said unplugged status detection unit, including resetting said unplugged status detection unit (Sedlak: column 3 lines 51-57).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sedlak in view of Selph et al. U.S. Pat. No. 4804957 (hereinafter Selph).

As per claim 2, Sedlak discloses a method according to claim 1. Sedlak does not explicitly disclose the step of re-initializing comprises determining at least one of said proper use and proper replacement of said security module by establishing communication between said first function unit and a remote data source exchanging information between said first function unit and said remote data source via current loop, and detecting that at least one of said proper use and proper replacement has occurred if said exchange of data takes place error-free.

However, Selph teaches that limitation (Selph: abstract and column 2 line 59 – column 3 line 34). It would have been obvious to one having ordinary skill in the art at the time of invention to combine the teachings of Selph within the system of Sedlak because it allows the erased data contents to be retrieved again in order to operate the security module.

7. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sedlak as applied to claim 3 above, and further in view of Higuchi U.S. Pat. No. 4823323 (hereinafter Higuchi).

As per claim 4, Sedlak discloses a security module as claimed in claim 3. Sedlak does not explicitly disclose said unplugged status detection unit comprises a line and switch element for resetting said self-holding capability, said switch element being triggered by a signal from said processor on said line. However, Higuchi teaches that limitation (Higuchi: column 2 line 38 – column 3 line27). It would have been obvious to one having ordinary skill in the art at the time of invention to combine the teachings of Higuchi within the system of Sedlak because it prevents abnormal operation of the CPU while power supply is replaced.

As per claim 5, the combination of Sedlak-Higuchi discloses a security module as claimed in claim 4, Sedlak does not explicitly disclose the limitation of claim 5. However, Higuchi discloses said unplugged status detection unit comprises: a voltage divider comprising a series resistor circuit connected across a terminal for receiving a supply voltage, tapped by a capacitor, and a line having a test voltage thereon (Higuchi: column 3 lines 3-10 and figure 1); a diode connected between said terminal for receiving a supply voltage and said capacitor (Higuchi: column 2 lines 12-47); a comparator having a non-inverting input, an inverting input

connected to a reference voltage source, and a comparator output (Higuchi: figure 2 and column 4 lines 56-64 and column 2 lines 12-16: the diode prevents inverse connection of the battery); a further capacitor tapping said voltage divider and connected to said non inverting input of said comparator (Higuchi: figure 2 and column 3 lines 3-10); said comparator output being connected to a line at a voltage potential via an inverter (Higuchi: figure 1 and column 4 lines 56-64); a switch element having a control input connected to said comparator output, said switch element producing said self-holding capability and being connected in parallel with a resistor of said voltage divider (Higuchi: figure 2: switch SW2); and said switch element for resetting said self-holding capability being connected between said voltage divider tap for said further capacitor, and ground (Higuchi: figure 2 and column 3 lines 3-10). It would have been obvious to one having ordinary skill in the art at the time of invention to combine the teachings of Sedlak and Higuchi because it is well known in the art to change the patterns of the circuits to make the chip suitable for many needs.

As per claim 6, the combination of Sedlak-Higuchi discloses a security module as claimed in claim 5. Sedlak does not explicitly disclose the limitations of claim 6. However, Higuchi discloses the security module further comprising an interrogation line connected between said processor and said unplugged status detection unit for interrogating a self-holding status of said unplugged status detection unit by said processor (Higuchi: figure 1: the voltage detector V1 and CPU). It would have been obvious to one having ordinary skill in the art at the time of invention to combine the teachings of Sedlak and Higuchi because it is inherent to connect the processor with the detection unit in order for the processor to function accordingly.

As per claim 7, Sedlak-Higuchi discloses a security module as claimed in claim 6. Sedlak further disclose said line having said test voltage thereon is at ground potential, and wherein said line at a voltage potential connected to said comparator output is at operating voltage potential when said security module is plugged into said device motherboard and is otherwise at ground potential when said security module is not plugged into said device motherboard (Higuchi: figure 1 and 2; column 3 lines 16-19; column 4 lines 56-64). It would have been obvious to one having ordinary skill in the art at the time of invention to combine the teachings of Sedlak and Higuchi because it allows the module to have self-holding capability.

As per claim 8, Sedlak discloses a security module as claimed in claim 3. Sedlak does not explicitly disclose the limitations of claim 8. However, Higuchi discloses said memory is contained in said processor and is at an operating voltage supplied from said voltage monitoring unit as long as said processor is supplied with system voltage, and wherein said processor has a terminal for resetting said self-holding capability of said unplugged status detection unit, and a further terminal for interrogating a status of said unplugged status detection unit (Higuchi: figure 1 and 2; column 3 lines 16-19; column 4 lines 56-64). Same rationale applies here as above in rejecting claim 7.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sedlak in view of Higuchi as applied to claim 8 above, and further in view of Mori et al. U.S. Pat. No.5039580 (hereinafter Mori).

As per claim 9, the combination of Sedlak-Higuchi discloses a security module as claimed in claim 8. Sedlak-Higuchi does not explicitly disclose the limitations of claim 9.

However, Mori discloses the security module further comprising an ASIC connected to said processor via an internal data bus, said ASIC having a first contact group for connection to a system bus of a device containing said device motherboard (Mori: figure 16 and column 13 lines 30-59: gate array). It would have been obvious to one having ordinary skill in the art at the time of invention to combine the teachings of Sedlak, Higuchi, and Mori because ASIC or gate array saves both design and manufacturing time by changing the pattern of connections to make the chip suitable for many needs.

9. Claims 10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sedlak as applied to claim 3 above, and further in view of Mori.

As per claim 10, Sedlak discloses a security module as claimed in claim 3. Sedlak does not explicitly disclose the limitations of claim 10. However Mori discloses a printed circuit board on which said processor, said voltage detector, and said unplugged status detection unit are mechanically and electrically mounted (Mori: figure 1-16; column 7 lines 47-58), said printed circuit board having contact terminals for a battery (Mori: figure 1-8; column 7 line 59 – column 8 line 24); a security module housing formed by a hard casting compound surrounding said printed circuit board and said processor, with said contact terminals being exposed to an exterior of said housing (Mori: figure 1-8; column 7 line 59 – column 8 line 24); a battery replaceably connected to said contact terminals outside of said housing (Mori: figure 1-8; column 7 line 59 – column 8 line 24); and said printed circuit board having a first contact group, accessible from outside of said housing, for communicating with a system bus of a device containing said device motherboard (Mori: figure 1,2, and 16; column 7 line 59 – column 8 line 24: the display), and a

second contact group accessible from an exterior of said housing for receiving system voltage (Mori: figure 1-8; column 7 line 59 – column 8 line 24: the battery compartment) and at least one of said first contact group and said second contact group being connected to said unplugged status detection unit to monitor a plugged status of said security module (Mori: figure 16: the display is connected with the CPU as disclosed by Mori while the CPU is connected with the voltage detection unit as disclosed by Sedlak). Mori does not explicitly disclose mounting said voltage detector and said unplugged status detection unit on the printed circuit board, but it would have been obvious to mount circuits with different capabilities on the same board. Therefore, it would have been obvious to one having ordinary skill in the art to combine the teachings of Mori within the system of Sedlak because mounting the processors and units on a printed circuit board allows more circuits with different capabilities to communicate better and faster as a whole.

As per claim 12, Sedlak discloses a security module as claimed in claim 3. However, Sedlak does not explicitly disclose said processor has a terminal for emitting at least one signal identifying a status of said security module. However, Mori discloses that limitation (Mori: figure 16 and column 13 lines 30-59). It would have been obvious to one having ordinary skill in the art at the time of invention to combine the teachings of Mori within the system of Sedlak because it is inherent for the processor to send a signal the display to identify the status of the security module.

As per claim 13, the combination of Sedlak-Mori discloses a security module as claimed in claim 12. Mori further discloses said processor is connected to an input/output unit having input/output ports, and having at least one internal signaling element in said security module

connected to said input/output ports (Mori: figure 16 and column 13 lines 30-59). Same rationale applies here as above in rejecting claim 12.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sedlak in view of Mori as applied to claim 11 above, and further in view of Higuchi.

As per claim 11, the combination of Sedlak-Mori discloses a security module as claimed in claim 10. Sedlak-Mori does not explicitly disclose said processor includes terminals for monitoring said plugged status of said security module with lines forming a current loop when said security module is plugged into said device motherboard. However, Higuchi teaches that limitation (Higuchi: figures 1 and 2; column 2 lines 38-64). It would have been obvious to one having ordinary skill in the art at the time of invention to combine the teachings of Sedlak, Mori, and Higuchi because the current loop allows the power source to be replaces without causing abnormal operation of the processor.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cutchis U.S. Pat. No. 5969504 discloses automatic battery power switch.

O'Connell et al. U.S. Pat. No.4903232 discloses electronic programmable stamping marking device.

Creta U.S. Pat. No. 6088762 discloses power failure mode for a memory controller.

Morino et al. U.S. Pat. No. 4805136 discloses program protection in a programmable electronic calculator.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shin-Hon Chen whose telephone number is (703) 305-8654. The examiner can normally be reached on Monday through Friday 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (703) 305-9648. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-3138.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Shin-Hon Chen
Examiner
Art Unit 2131

SC

EMMANUEL L. MOISE
PRIMARY EXAMINER